

FIG. 1

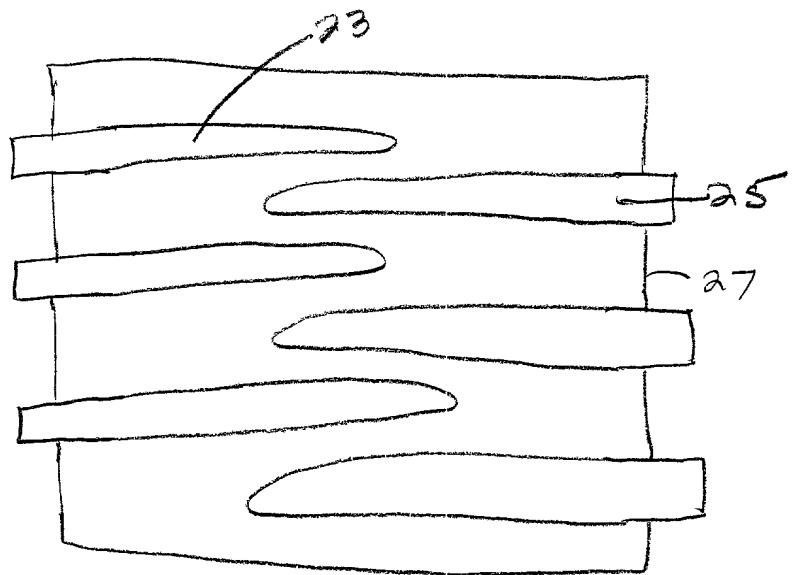


FIG. 2A

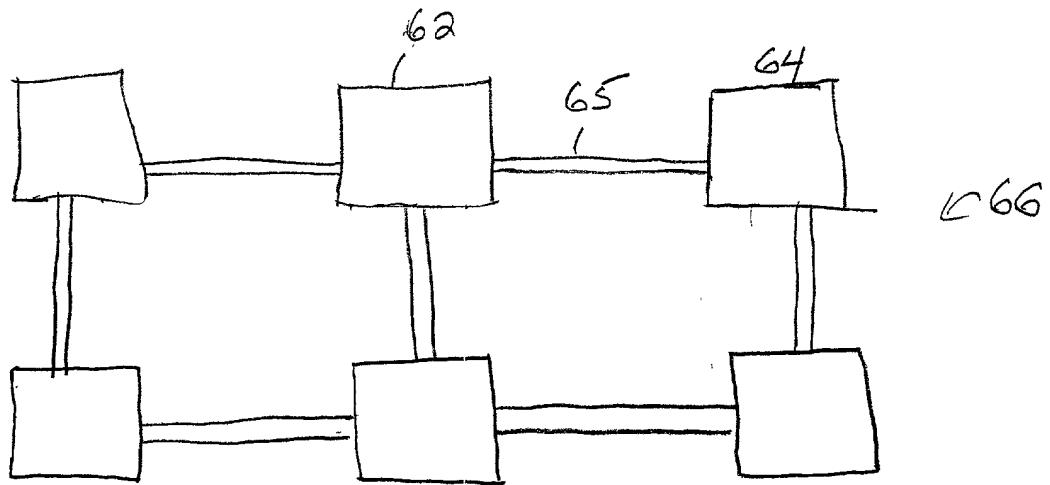


FIG. 5

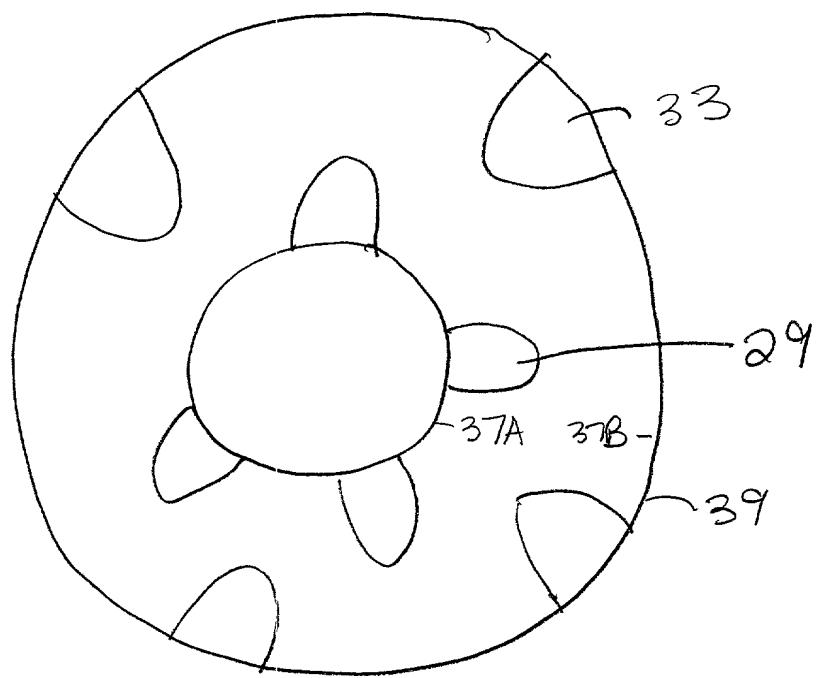


FIG. 2B

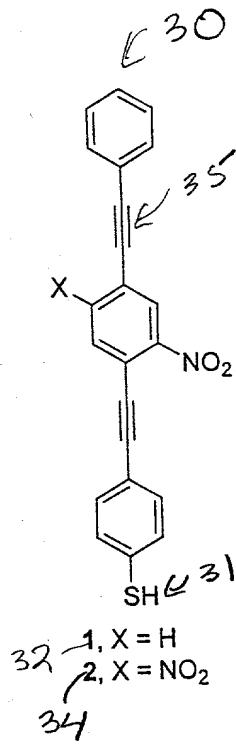


FIG. 3

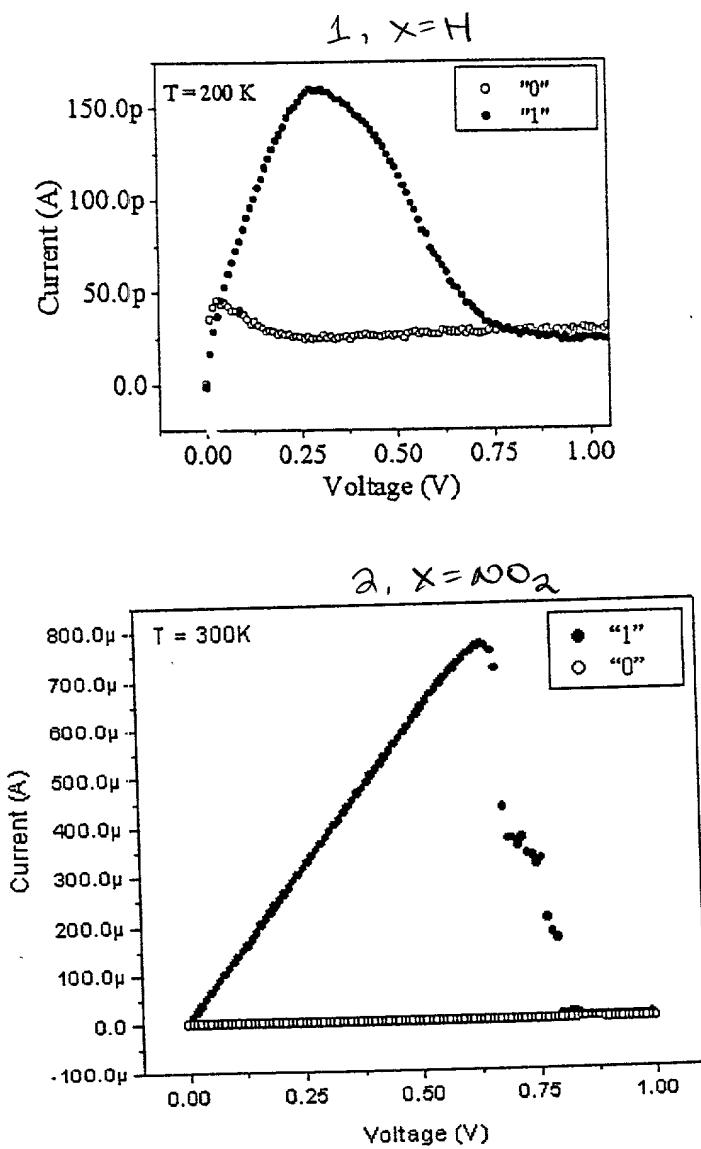


FIG. 4

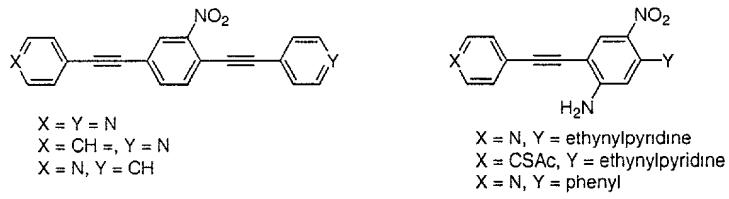


FIG. 6

## Untrained Nanocell

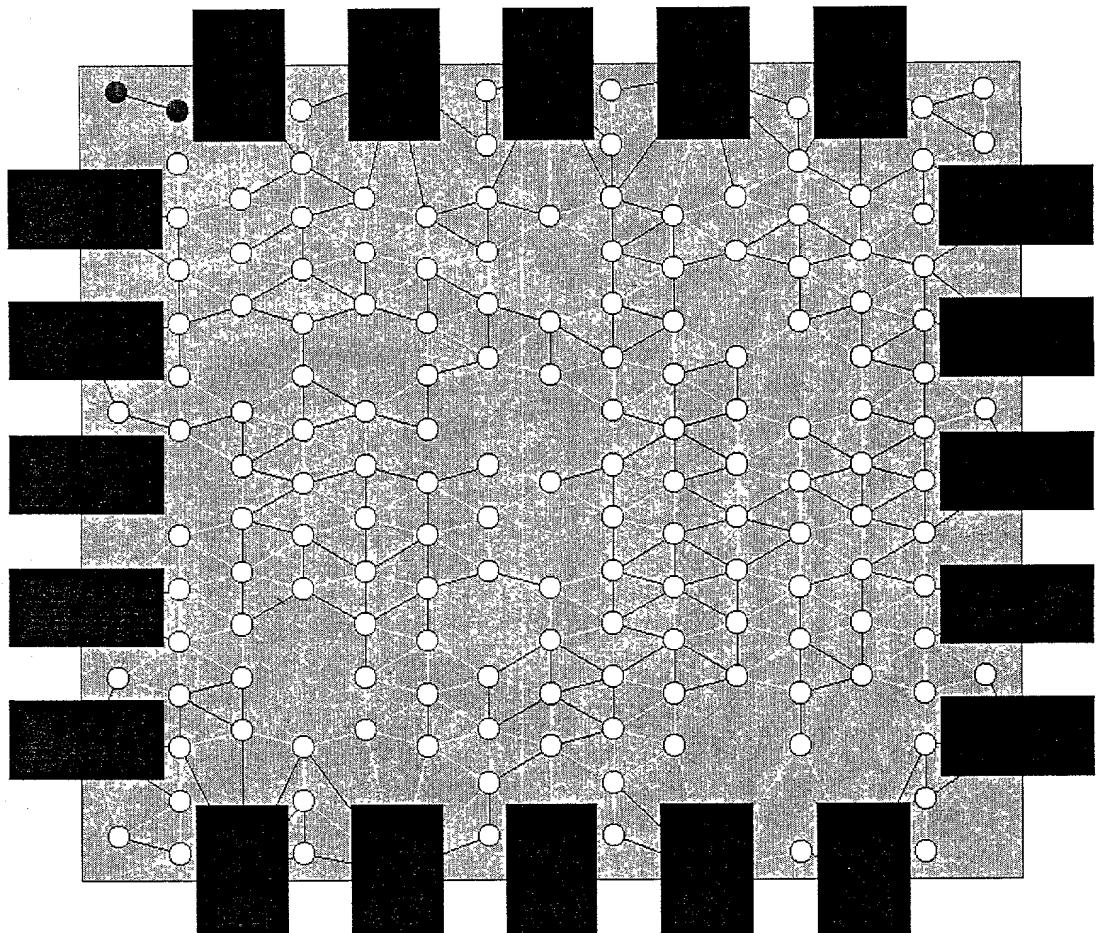
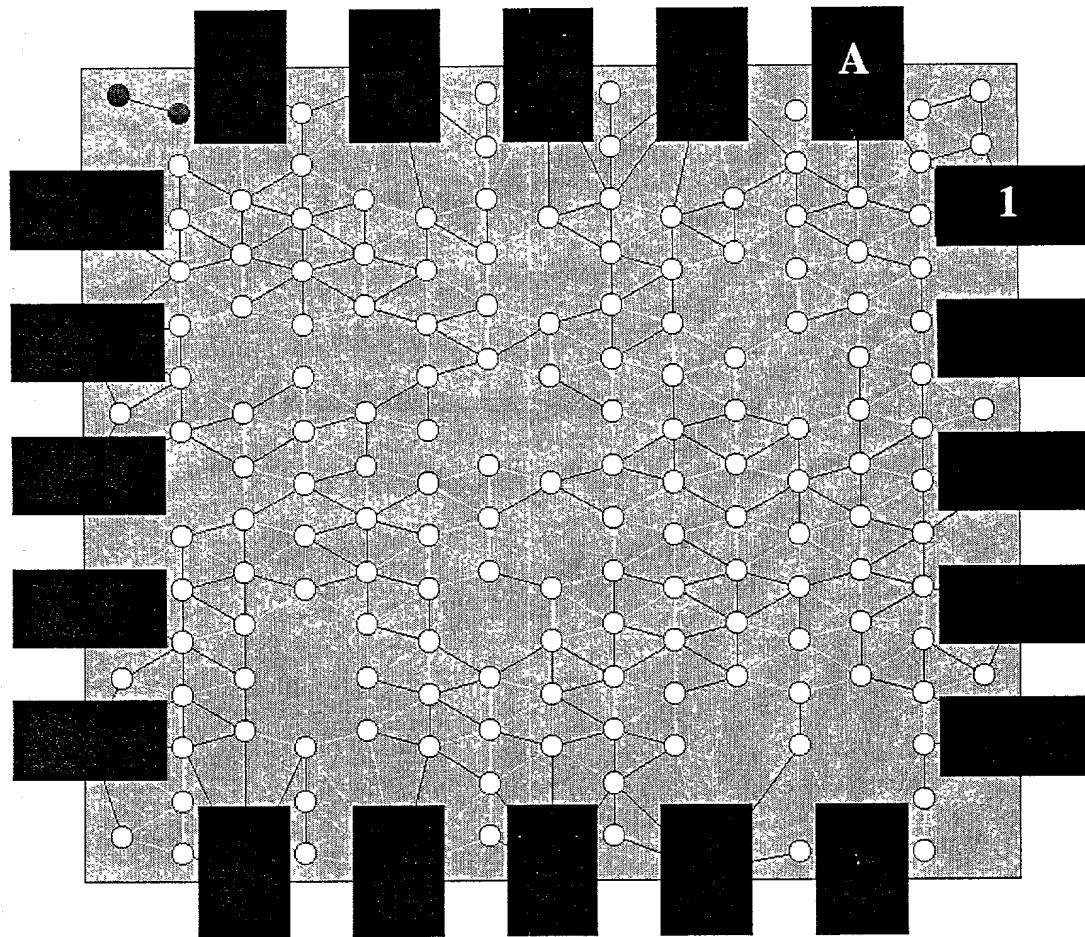


FIG. 7

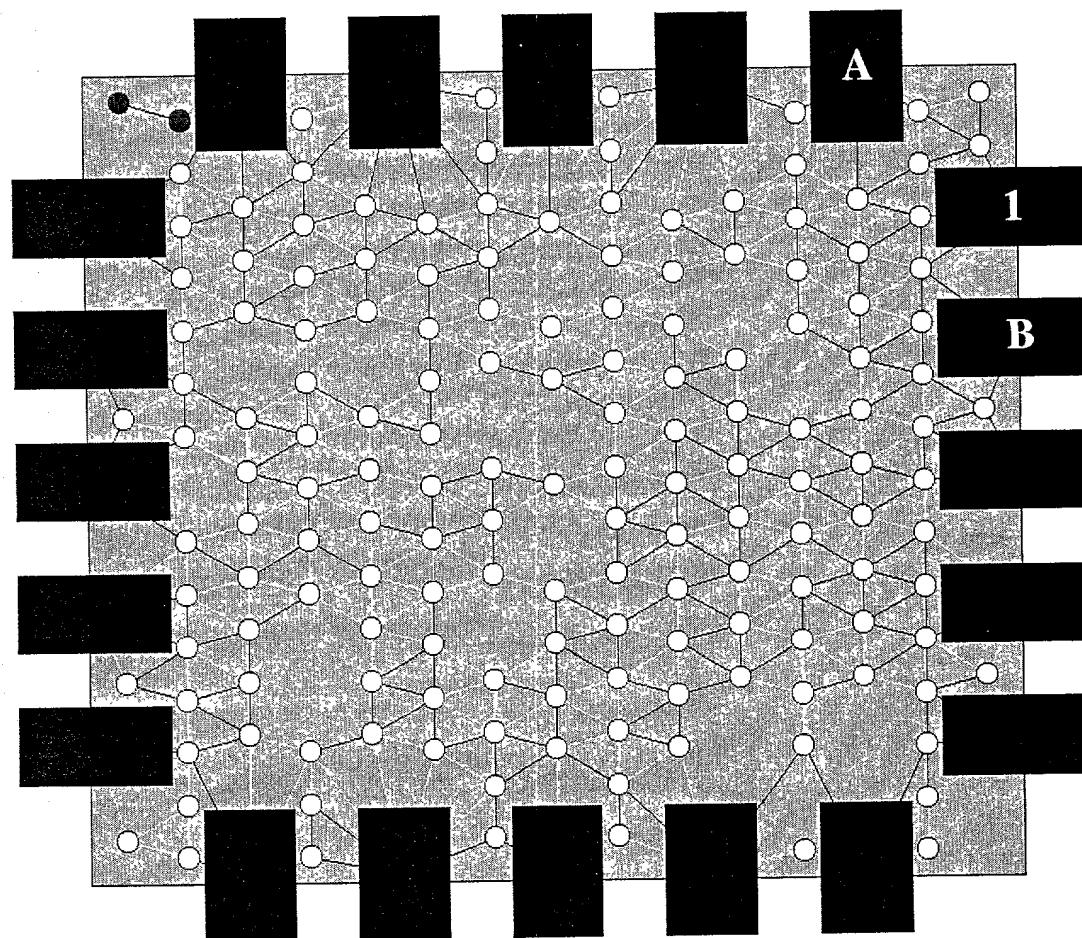
## Nanocell Trained as Inverter



Inverter Truth Table	
Input A	Output 1
0	1
1	0

FIG. 8

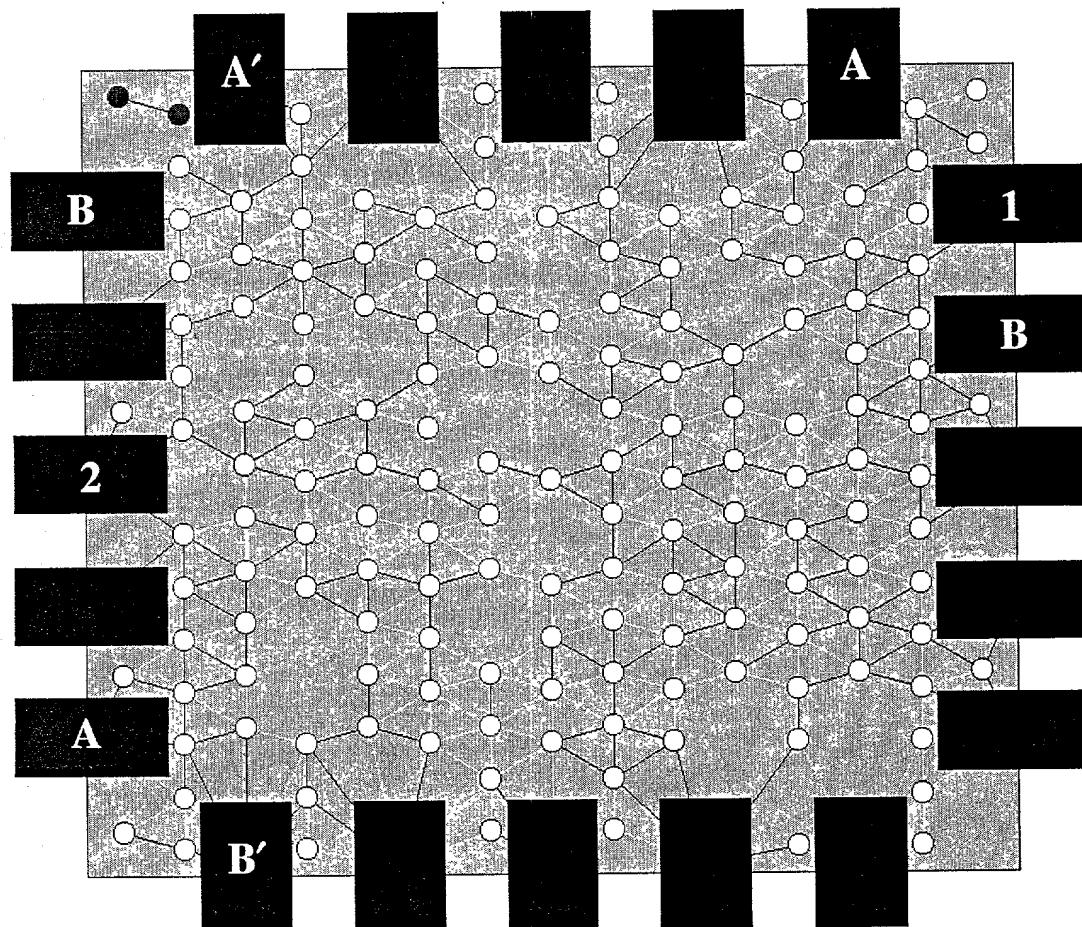
## Nanocell Trained as Nand



Nand Truth Table		
Input A	Input B	Output 1
0	0	1
0	1	1
1	0	1
1	1	0

FIG. 9

## Nanocell Trained as Inverse Half Adder



Inverse of Half Adder Truth Table			
Input A	Input B	Output 1	Output 2
0	0	1	1
0	1	1	0
1	0	1	0
1	1	0	1

FIG. 10